Report Draft for Comp Org P3

Using Python 3.6 for code.

Started by implementing the 1KB, DM, block size 8 cache. Didn’t care about write policy in beginning. Made functions for building the cache, writing to, and reading from the cache. Tracked hits. Once this was working, made a loop to go through the different cache sizes. Once this worked, began working on implementing different cache placement policies.

Use random LRU replacement policy. When writing to a 2W, 4W, or FA cache, the line at the specified tag will be randomly chosen. We will check for hit/miss at this chosen line, and write to the chosen line

When reading from one, we need to loop through all of the possibilities and check each tag and valid bit. If at least one of those is good, we’ll return a hit. Otherwise, return a miss